WHAT IS CLAIMED IS:

1. A method of fabricating a non-volatile memory device comprising:

forming a lower conductive layer on a substrate;

forming a lower and an upper sacrificial patterns on the substrate, wherein the lower and upper sacrificial patterns include a trench exposing the lower conductive layer;

forming mask spacers on sidewalls of the upper and lower sacrificial patterns;

etching the exposed lower conductive layer to form a lower conductive pattern exposing the substrate by using the mask spacers and the upper sacrificial pattern as an etch mask;

forming a plug conductive layer covering an entire surface of the substrate with the lower conductive pattern; and

planarizing the plug conductive layer until the lower sacrificial pattern is exposed, thereby forming a source plug connected to the exposed substrate in a gap region between the mask spacers.

2. The method of claim 1, before forming the lower conductive layer, further comprising:

forming a device isolation layer in a predetermined region of the substrate; and

forming a gate oxide layer covering the active region, wherein the lower conductive layer is parallel to the active region and covers the gate oxide layer.

3. The method of claim 1, wherein said step of forming the upper and lower sacrificial patterns further comprises:

sequentially forming a lower and an upper sacrificial layers on the substrate with the lower conductive layer; and

successively patterning the upper and lower sacrificial layers to form a trench that exposes the lower conductive layer and crosses over the active region.

4. The method of claim 3, wherein the forming the trench is performed by anisotropic etching process to round a top portion of the exposed lower conductive layer exposed through the trench.

5. The method of claim 1, wherein the lower sacrificial pattern is a silicon nitride.

6. The method of claim 1, wherein the upper sacrificial pattern and the mask spacers include a different material from the lower sacrificial pattern.

7. The method of claim 1, wherein the upper sacrificial pattern is a

silicon oxide.

8. The method of claim 1, further comprises forming an impurity region serving as a source in the exposed substrate, after forming the lower conductive pattern.

9. The method of claim 1, further comprises forming an oxide layer or a nitride layer that covers sidewalls of the lower conductive pattern, before forming the plug conductive layer.

10. The method of claim 1, after forming the source plug, further comprising:

forming floating gates under the mask spacers; and

forming control gates beside the floating gates.

11. The method of claim 10, before forming the floating gate, further comprising:

forming an etch stop insulation layer on the source plug; and

removing the exposed lower sacrificial pattern to expose the lower conductive pattern.

12. The method of claim 11, wherein said step of forming the floating gate comprises anisotropically etching the exposed lower conductive pattern using the mask spacers as an etch mask.

13. The method of claim 10, before forming the control gate, further comprising:

forming sidewall insulation layers interposed between the floating gates and the control gates.

14. The method of claim 13, wherein the sidewall insulation layers are formed by thermally oxidizing the sidewalls of the floating gates.

15. The method of claim 10, wherein said step of forming the control gates further comprises:

stacking an upper conductive layer on an entire surface of a substrate with the floating gates;

planarizing the upper conductive layer to form an upper conductive pattern disposed beside the floating gates; and

patterning the upper conductive pattern to cross over the active region.

16. The method of claim 10, after forming the control gate, further comprising:

forming impurity region serving as a drain in a substrate beside the control gates.

17. The method of claim 1, wherein said step of planarizing the plug conductive layer uses a chemical mechanical polishing process.

18. The method of claim 1, wherein said step of planarizing the plug conductive layer uses an etch recipe having a selectivity with respect to the upper sacrificial pattern.

19. The method of claim 1, wherein the upper sacrificial pattern is formed having a thickness of about 200 to about 3000Å.

20. A method of fabricating a non-volatile memory device comprising:

forming a conductive layer on a substrate;

forming a first and a second sacrificial patterns on the substrate;

etching the first and second sacrificial patterns to form a trench and expose a top surface of the conductive layer;

forming mask spacers on sidewalls of the trench;

etching the exposed conductive layer to form a lower conductive

pattern and expose the substrate by using the mask spacers and the second sacrificial pattern as an etch mask;

forming a plug conductive layer filling the trench with the mask spacers and connecting to the exposed substrate; and

planarizing the plug conductive layer until the first sacrificial pattern is exposed to form a source plug connected to the exposed substrate.